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Research on Design Technology of High Efficiency Boost DC-DC Converter with Wide Load Range

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Abstract

In order to solve the problem of low conversion efficiency of traditional DC-DC switching power supply under light load, this paper adopts the combination of zero crossing detection technology and pulse width modulation (PWM)/skip period modulation (PSM) automatic switching technology through in-depth study of the source of power loss. The conversion efficiency under different loads is improved. On the one hand, through the zero crossing detection technology, when the inductance current drops to zero, the intermittent current tube is turned off in time to prevent the current from flowing back to the power supply and causing energy loss; On the other hand, PSM is used to skip part of the cycle to reduce the working frequency, that is, to reduce the switching loss and drive loss, improve the conversion efficiency of the system, and solve the problem of low efficiency of DC-DC switching power supply at light load. Based on the 0.18 μm BCD process completes the physical implementation and test verification of the proposed method. The test results show that when the input voltage is 3.7 V and the output voltage is 4.6 V, the system can achieve smooth switching between PWM mode and PSM mode, and can timely turn off the intermittent current tube when the inductance current crosses zero. The highest efficiency can reach 97% and the lowest efficiency can reach 92.22% in the full load range of 10 mA-900 mA.

Keywords

DC-DC switching power supply; over-zero detection; PWM/PSM automatic switching; high efficiency.

1. INTRODUCTION

With the growth of portable electronics,there is an urgent need for new power supplies and power management integrated circuits with high efficiency, high current loads and high frequency.dc-dc converters are becoming very important[1].literature[2]Adopts PWM/PFM hybrid mode automatic switching technology with a load range of 10 mA-300 mA, which utilizes simple control logic and comparator propagation delays to determine the mode change point, with a simple structure and a conversion efficiency of up to 97 %.literature[3]uses PWM/PSM auto-switching to achieve high conversion efficiency within full load, but it has a slightly complex logic control circuit and excessive ripple.literature[4]Using PWM and PFM automatic switching modes over the full load range, the system has a recovery time of 3.3 μs from a full load of 1 A to a light load of 10 mA. Efficiency of 80% or more can be achieved over the 10 mA-1 A load current range. Has a fast transient response, but light load efficiency is too low.Literature [5] uses PWM+PFM technique and the conversion efficiency is more than 85 % and up to 96 % in 2 mA-500 mA load current range. The efficiency is high at heavy loads, but the load range is small and it requires the use of bypass switches and a complex circuit

ISSN: 2472-3703 DOI: 10.6911/WSRJ.202503_11(3).0014

structure.Literature [6] uses a minimum duty cycle module to realize smooth switching of PWM/PSM with simple circuit control. However, the conversion efficiency is more than 75 % in the load range 10 mA-1 A. The light load efficiency is too low.

For the above problems, this paper proposes a combination of over-zero detection technology and PWM/PSM automatic switching technology. Through simple logic control, the system works in PWM mode when a high current load is detected, and in PSM mode when a low current load is detected, and the over-zero detection circuit starts to work to improve the efficiency of the system within a wide load.

2. POWER LOSS ANALYSIS

DC-DC converter losses are mainly conduction losses, switching losses, driving losses and static losses. The power loss of the converter is the difference between the input power and the output power, and the conversion efficiency of the system is defined as the ratio of the output power Pout to the input power Pin, and the expression is:

$$\eta = \frac{P_{out}}{P_{in}} = \frac{V_{out} \bullet I_o}{V_{in} \bullet I_{in}} \tag{1}$$

Where V_{out} is the output voltage of the system and I_o is the load current,V_{in} is the input supply voltage， I_{in} is the input current.

2.1. Conduction loss

Power tubes have on-resistance, when the circuit works normally, the current flows through the power tube will produce conduction loss. The conduction loss can be expressed as:

$$P_{CON} = I_{RMS}^{\ 2} \bullet R_{ON} \tag{2}$$

Where R_{ON} represents the on-resistance of the power tube and I_{RMS} represents the root-mean-square current flowing through the power tube, which is divided into DC and AC parts, and is expressed as:

$$I_{RMS}^{\ 2} = I_{RMS(AC)}^{\ 2} + I_{RMS(DC)}^{\ 2} \tag{3}$$

$$I_{RMS(AC)}^{\ 2} = D \bullet \frac{\Delta I^2}{12} \tag{4}$$

$$I_{RMS(DC)}^{\ 2} = D \bullet I_O^{\ 2} \tag{5}$$

When the input voltage and output voltage is certain, the inductor current ripple and duty cycle is fixed, on behalf of the AC current generated by the on-state loss is fixed, while the DC current generated by the on-state loss is proportional to the square of the load current. The on-state loss is proportional to the component on-state resistance R_{ON}, and the on-state resistance expression is:

$$R_{ON} = \frac{1}{\mu_n C_{ox} \frac{W}{L} (V_{GS} - V_{TH})} \tag{6}$$

ISSN: 2472-3703 DOI: 10.6911/WSRJ.202503_11(3).0014

From the expression it can be seen that increasing the gate source voltage V_{GS} of the power tube reduces the conduction loss.

2.2. Switching Loss

Gate drive signal in the periodic switching action, the current flowing through the power tube is not zero, and the gate voltage of the power tube has a certain rise and fall time, resulting in energy loss on the power tube, known as switching loss. The formula is:

$$P = \frac{I_{MAX} \bullet t_r + I_{MIN} \bullet t_f}{6} \bullet V_{IN} \bullet f \tag{7}$$

Where I_{MAX} and I_{MIN} are the maximum and minimum currents flowing through the power tube.t_r and t_f are Rise and fall times of power tube gate drive signals， V_{IN} is the input voltage of the system， f is the switching frequency.

2.3. Driving Losses

The drive loss is mainly due to the charging and discharging of the gate capacitance of the power tube by the periodic drive signal, which is expressed as:

$$P_{\text{gate}} = C_{gate} \bullet f \bullet V_{IN}^{2} \tag{8}$$

Where, Cgate represents the gate capacitance, which consists of gate source capacitance, gate drain capacitance, drain liner capacitance and gate oxide capacitance. f represents the switching frequency, and VIN is the input supply voltage.

2.4. Static loss

Static loss is the power consumption generated by the bias current, called static power consumption, which is unavoidable in the circuit when the DC-DC converter module circuit operates normally. Its expression is:

$$P_Q = V_{IN} \bullet I_Q \tag{9}$$

Where V_{IN} is the supply voltage, I_Q is the quiescent current, it can be seen that reducing the quiescent current and supply voltage can reduce the quiescent loss. When designing the circuit, the circuit structure can be simplified to avoid excess quiescent current consumption. The quiescent current is of microampere level, which is negligible under heavy load. However, under light load, the quiescent current is not small enough to be ignored.

In summary, the power tube conduction loss is proportional to the square of the load current, as the load current increases, the proportion of greatly increased. Switching loss and driving loss has nothing to do with the load current, and switching frequency is proportional to the higher frequency loss, the lighter the load power tube switching loss and driving loss in the overall loss accounted for the proportion of the larger, resulting in light load conversion efficiency is low[7-8].Therefore, in order to improve the conversion efficiency under light load, this paper adopts the cycle-skipping modulation PSM method at light load to skip some cycles and reduce the switching frequency to improve the efficiency.

ISSN: 2472-3703 DOI: 10.6911/WSRJ.202503_11(3).0014

3. OVERALL LOOP ARCHITECTURE

In this paper, the overall architecture of DC-DC switching power supply with boost-type peak current mode control is shown in Fig.1, and the control circuit consists of resistive feedback network, EA error amplifier, PWM comparator, PSM comparator, logic gate circuit, RS flip-flop, FREE_dete over-zero detection circuit and Digital circuit digital circuit.

The principle of operation is: because the output of the error amplifier is proportional to the load current, as the load current decreases, the V_C value also decreases, so set the V_d value in advance equal to the V_{SIGMA} value corresponding to the load current I_O in the critical conduction mode.

When the system works in high current load, PSM comparator in-phase terminal is larger than the inverse terminal, after the logic gate circuit finally outputs a low level of 0 V, will not have an impact on the PWM, the whole system is still working in the PWM mode.At light load, the output value of the error amplifier V_C is less than V_d, at this time, the PSM comparator outputs a high level of 1 V, after the and non-gate to shield the output signal of the PWM comparator, at this time, the system operates in the PSM mode.Moreover, the PSM mode has a self-wake-up function, when a light load is detected, the power tube gate control signal begins to skip part of the cycle, at which time the output voltage V_{out} begins to fall, then the error amplifier output voltage V_C begins to rise, and when it rises to a value greater than the V_d value, the control loop generates a periodic switching action on the main switch tube and the continuity tube, which ultimately causes the output voltage V_{out} to rise to its original value.

In addition, in order to further improve the efficiency of light load, this paper also sets the over-zero detection circuit, inductance current in the decline to zero, shut down the continuity tube, cut off the output to the input path, to avoid the occurrence of inductance current backflow. The specific principle is: compare LX1 and V_{out} value, in the renewal stage output voltage value V_{out} is greater than the LX1 point voltage, through the logic circuit output high level, timely shutdown of the continuous flow tube M_2.

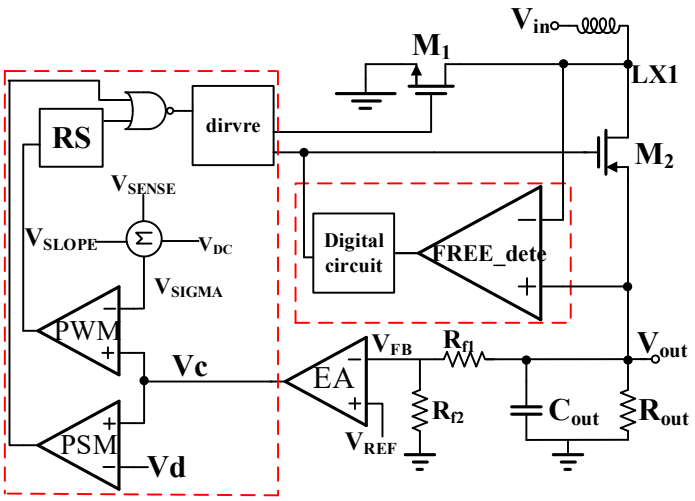


Figure 1. Schematic diagram of DC-DC switching power supply with boost peak current mode control

4. THE INDUCTOR CURRENT OVER-ZERO DETECTION CIRCUIT PROPOSED IN THIS PAPER

In order to prevent the inductor current from backing up during the renewal stage, this paper designs an over-zero detection circuit, as shown in Fig. 2. Mainly by comparing the voltage LX1 and V_{out} at the two ends of the continuity tube, when $V_{LX1}>V_{out}$, the over-zero signal X_1' outputs

ISSN: 2472-3703 DOI: 10.6911/WSRJ.202503_11(3).0014

a low level, and the over-zero detection circuit does not affect the operating state of the system. When $V_{LX1} < V_{out}$, the over-zero signal X_1'output high level, after the logic circuit to determine whether in the renewal stage, if at this time in the renewal stage, the logic signal to immediately shut down the renewed tube, thereby reducing the power loss of the system. In addition, but also consider the logic circuit there is a certain delay time, in the design of the circuit to take the delay time into account, so the circuit needs to retain a certain margin, so that the inductor current is about to reach zero, shut
down the continuity of the tube in a timely manner.

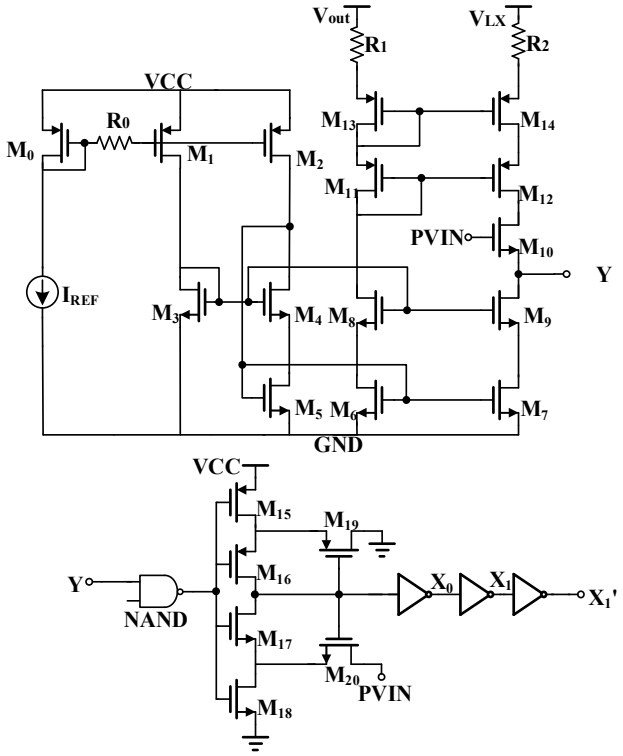


Figure 2. Zero crossing detection circuit structure diagram

M_6-M_{14} and resistors R_1 and R_2 form the voltage comparator, and the non-gate, Schmitt trigger and inverter form the shaping circuit. Among them, M_0-M_9 constitute the current bias circuit, providing the reference current I_{REF} for the circuit. resistors R_1 and R_2 are used to adjust the threshold value of the control signal flip-flop in advance ΔV. Since the MOS tubes M_{13} and M_{14} are connected to the gate and the source potential is different, the current size of the two branches will have the source potential to decide. The specific operation principle of the over-zero detection circuit is: when $V_{out}>V_{LX1}$, M_{13} source voltage is greater than the source voltage of M_{14}, at this time, $V_{GS13}>V_{GS14}$, then the Y-point pull-down current is greater than the pull-up current, the Y-point potential is pulled down, through the logic gate circuit shaping X_1' output high level. When $V_{out}<V_{LX1}$, the source voltage of M_{13} is smaller than the source voltage of M_{14}, at this time $V_{GS13}<V_{GS14}$, the pull-up current of Y point is larger than the pull-down current, the potential of Y point is pulled up, and the logic gate circuit shaping X_1' outputs a low level. In order to prevent Vout from repeatedly flip-flopping around V_{LX1}-ΔV, resulting in a chaotic output signal, a Schmitt trigger is added to the logic control output circuit. The size of the threshold ΔV is:

$$\Delta R = R_2 - R_1 \tag{10}$$

$$\Delta V = \Delta R \bullet I_{REF} \tag{11}$$

ISSN: 2472-3703 DOI: 10.6911/WSRJ.202503_11(3).0014

From the formula it can be seen that changing the size of R_1 and R_2 can obtain different thresholds. Over-zero detection circuit can be in the output voltage is greater than the LX1 point voltage, the output high level to switch off the continuity tube, but also need additional logic control circuit Figure 3 to determine when $V_{out}>V_{LX1}$, the circuit is in the charging stage or the continuation stage, only in the continuation stage can switch off the continuity tube.

As shown in Figure 3 below, the logic circuit function of the boxed out part is to screen out the continuation of the current state, and again the inductor current over zero. Specific operating principle: the main switching tube gate signal N1_G for the enable signal, when the system is in the charging stage that is, N1_G is high, the enable signal works, the output signal Q 'direct low 0 V. When the system is in the continuation stage, that is, N1_G is low, the enable signal does not work, only as an input signal, the circuit constitutes a master-slave rising edge Trigger. At this time to analyze the circuit's over-zero signal X_1', when X_1' for the low level inductor current did not cross zero, the output signal Q'maintenance; when X_1' for the high level inductor current over zero, the output signal Q'high level. The circuit screens the inductor current over zero state in the renewal phase. X_A2 signal is the waveform of the main switching signal after the inverter delay and Schmitt trigger shaping, in order to eliminate the falling delay of the over zero signal X_0 through the Schmitt trigger.

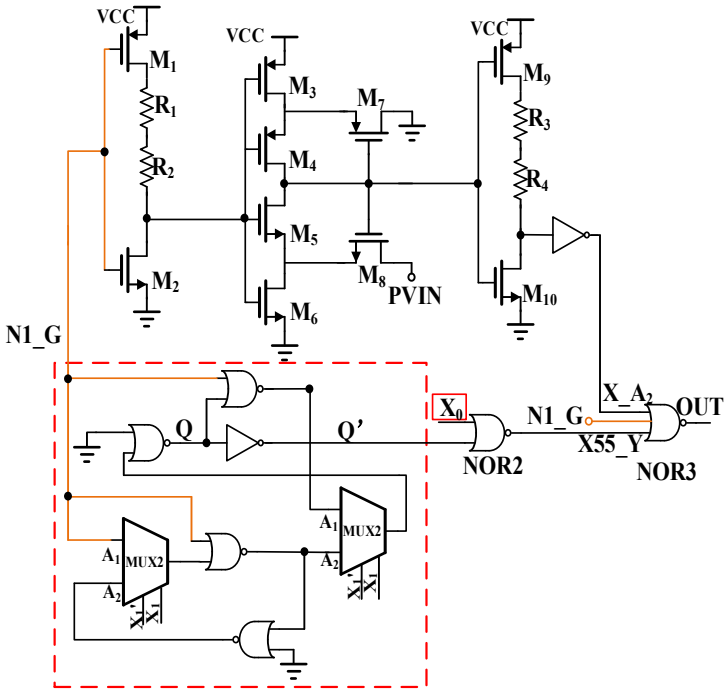


Figure 3. Logic control output circuit

The or non-gate NOR2 and NOR3 screen out the inductor current over-zero signal to avoid misjudgment of the circuit. The principle of realization is as follows: in the charging stage N1_G is high and the output signal OUT is low, which does not affect the working state of the system. In the renewal phase N1_G and X_A2 is low, if the inductor current is detected over zero X_0 is high, that is, the output signal OUT is high level shutdown of the renewable tube, to prevent the inductor current back-up; if it is not detected over zero X_0 for a low level, then the Q' is also low, that is, X55_Y is high, through the or non-gate NOR3 output signal OUT for a low level, does not affect the system operating state. low level, does not affect the operating state of the system. In summary, the logic control output circuit can be in the renewal stage inductor current exceeds zero, timely shutdown of the continuity tube to prevent power loss.

ISSN: 2472-3703 DOI: 10.6911/WSRJ.202503_11(3).0014

5. THE PWM/PSM ADAPTIVE SWITCHING METHOD PROPOSED IN THIS PAPER

Due to the high efficiency of PWM mode heavy load and PSM light load efficiency characteristics, this paper specially designed a PWM/PSM automatic switching circuit shown in Figure 4, can be realized in light load, the circuit works in PSM mode, skipping part of the cycle to reduce the switching frequency, reduce switching losses and drive losses, improve system efficiency. While in heavy load, from the power loss analysis, it can be seen that the conduction loss accounts for the largest proportion, which is proportional to the square of the load current, suitable for PWM mode. PWM/PSM automatic switching technique is used to achieve high efficiency under full load.

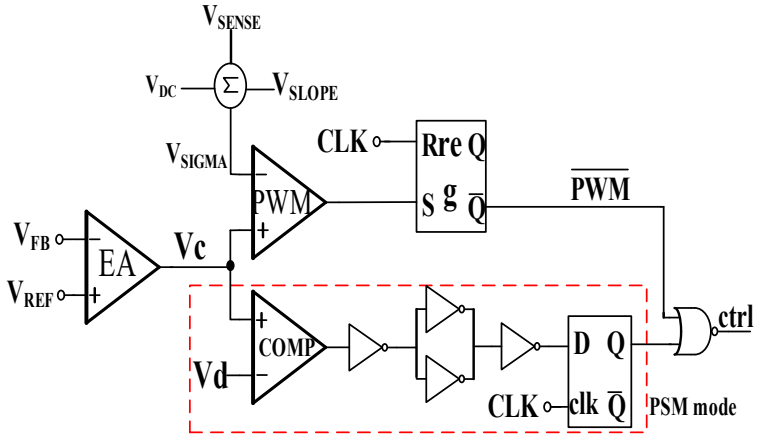


Figure 4. Circuit diagram of PWM/PSM automatic switching

The specific switching principle is as follows: under heavy load, the circuit works in PWM mode. When the system enters the light load, the circuit from the continuous conduction mode CCM into the discontinuous conduction mode DCM, the output voltage V_{out} began to rise, then the feedback voltage V_{FB} followed by a rise, at this time, $V_{FB}>V_{REF}$, the error amplifier EA's output voltage V_C down, when down to less than the fixed voltage V_d, PSM comparator module after the final output of the logic gate for the high level, then the PWM signal does not work, during this period will skip a few cycles and work in the PSM mode. signal does not work, in the meantime will skip a few cycles, and work in PSM mode. Until the output voltage Vout falls, the error amplifier EA output voltage V_C begins to rise, the circuit's self-wake-up mode. V_d is the V_{SIGMA} value corresponding to the load current I_O in the critical conduction mode, and the value of the critical conduction mode load current is determined by the following equation:

$$I_{av} = \frac{I_o}{1-D} \tag{12}$$

$$\Delta I_{L-} = \frac{V_{\text{in}} - V_{out}}{L} \bullet (1-D) \bullet T \tag{13}$$

Where I_{av} is the average value of inductor current, D is the duty cycle, V_{in} is the supply voltage, V_{out} is the output voltage, T is the system operating period and L is the inductor. After mathematical operation, the load current value I_o in critical conduction mode is 40 mA, so when the load current value I_o<40 mA, the system enters the discontinuous conduction mode, working in the hopping cycle modulation, when the load current value I_o>40 mA, the system enters the continuous conduction mode, working in the PWM mode.

ISSN: 2472-3703 DOI: 10.6911/WSRJ.202503_11(3).0014

6. EXPERIMENTAL RESULTS AND DATA ANALYSIS

In this paper, the physical layout of the proposed circuit is designed and fully simulated based on the 0.18 μm BCD process. Fig. 5 shows the actual layout photo of the Boost converter chip, and the overall area of the chip is 1469 μm×1180 μm, of which the area of the over-zero detection module is 332 μm×201 μm, and the area of the PSM module is 134 μm×50 μm,. The supply voltage range of this converter is 2.9 V~4.5 V and the load current range is 10 mA~900 mA.

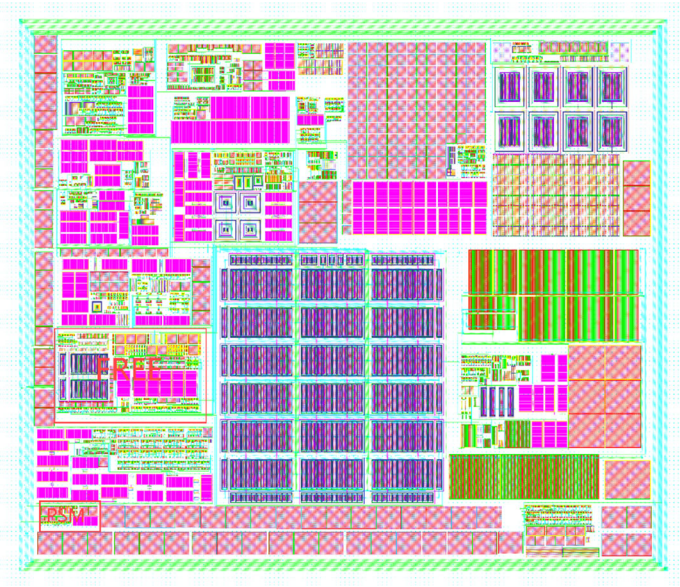


Figure 5. Photo of overall layout of chip

When the load current is greater than 50 mA, the system operates in continuous conduction mode and no backflow of inductor current occurs, indicating that the over-zero detection circuit does not have any effect on the system under a high current load. Therefore, in order to compare the effect of the over-zero detection circuit on the system, it is only necessary to analyze the system operating at a small current load.

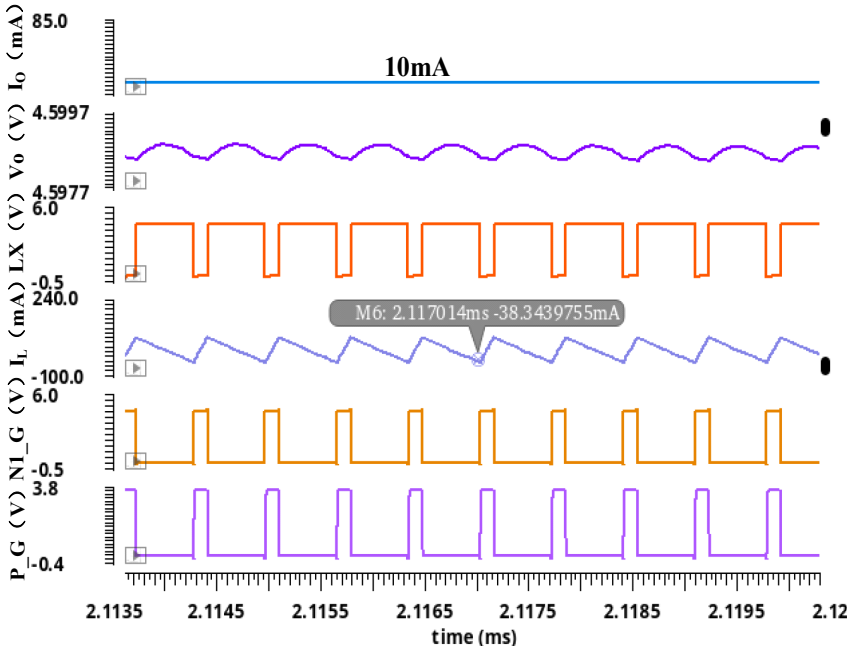


Figure 6. Simulation waveform without zero crossing detection

ISSN: 2472-3703 DOI: 10.6911/WSRJ.202503_11(3).0014

The above Fig.6 shows the simulated waveform of the circuit without over-zero detection. Where I_O represents the load current, V_o represents the output voltage, LX represents the node voltage, N1_G represents the gate voltage of the main switching tube, I_L represents the inductor current, and P_G represents the gate voltage of the continuator. From the figure, it can be seen that the system under light load, the inductor current I_L drops to -38 mA after crossing zero, indicating that at this time a path from the output voltage to the input voltage is formed, and the inductor current backflow phenomenon occurs, resulting in energy loss.

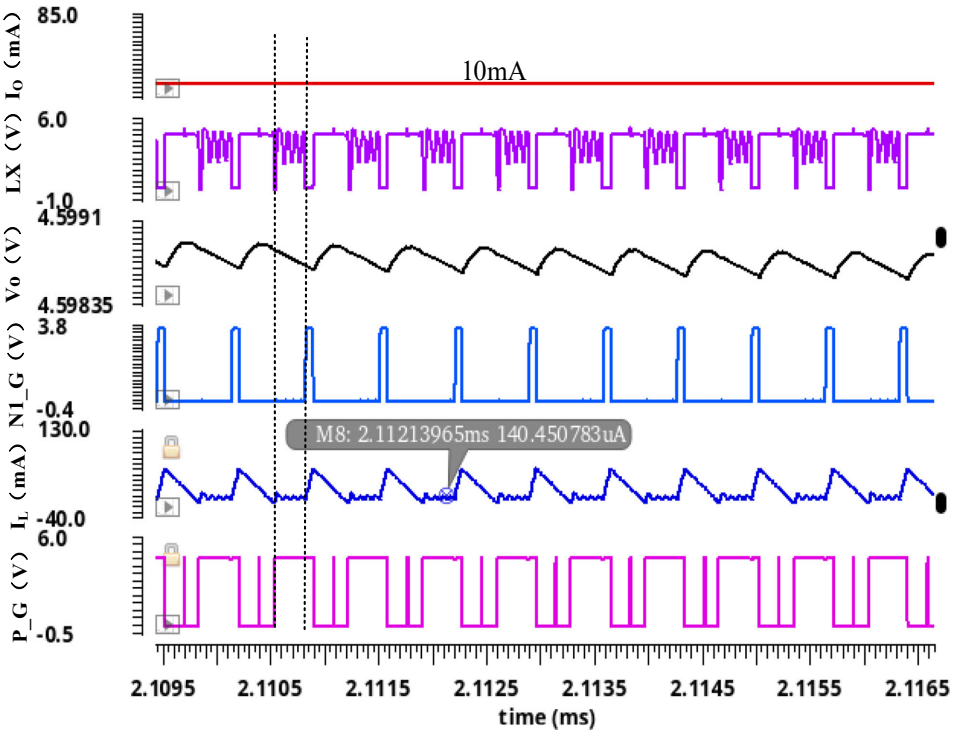


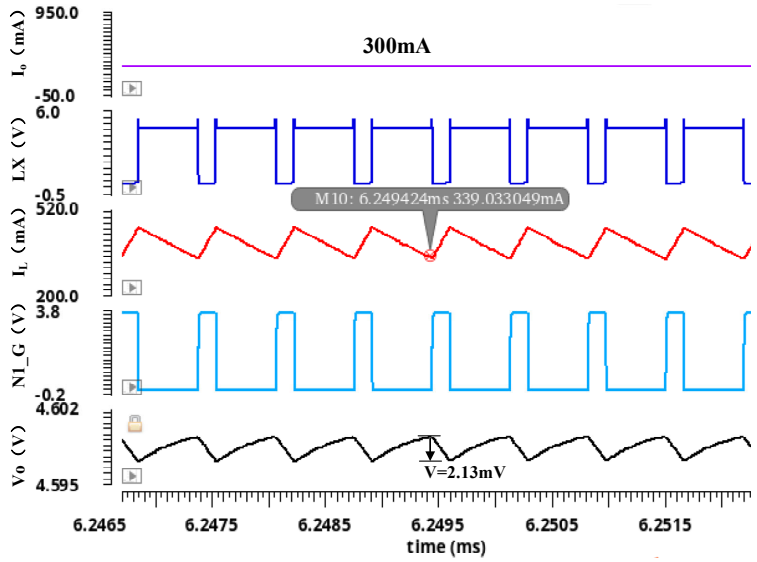
Figure 7. Simulation waveform of zero crossing detection

Fig.7 shows the simulation diagram of the addition of the over-zero detection circuit, which can be seen in the figure between the two labeled lines,, the main switch gate signal N1_G is a low level, the system is in the renewal phase, at this time, $V_{out}>V_{LX}$, the refill tube gate signal P_G is a high level, the inductor current I_L to zero after not continue to fall, but fluctuations in the vicinity of 140 μA. This indicates that the over-zero detection module detects the inductor current over-zero in the renewal stage, and outputs a high level to turn off the continuity tube in time, avoiding the energy loss caused by the backflow of the inductor current and improving the conversion efficiency of the system.

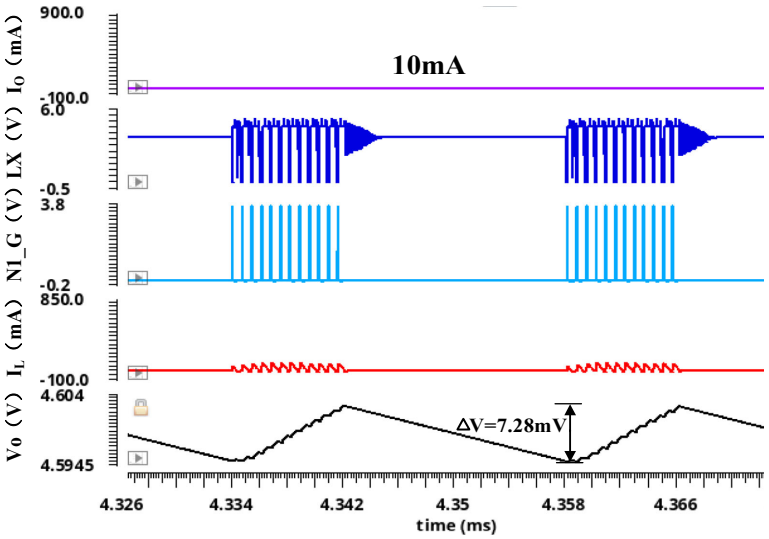
Fig.8 shows the overall simulated waveforms of the system with the addition of over-zero detection and PSM, from Fig. (a), it can be seen that the system operates in PWM mode at a load current I_O=300 mA, the inductor current drops to 339 mA and then rises after that, and it is in continuous conduction mode with a ripple voltage of 2.13 mV.

At light load I_O=10 mA, the system works in DCM mode in Fig.(b), the switching node LX produces normal resonance phenomenon, and the main switching tube skips part of the cycle, which reduces the switching frequency, the switching and driving losses are reduced, and the efficiency is improved. However, the ripple voltage also becomes 7.28 mV, and the ripple characteristics become worse.

ISSN: 2472-3703 DOI: 10.6911/WSRJ.202503_11(3).0014



(a) Heavy duty



(b) Light load

Figure 8. Overall simulation waveform

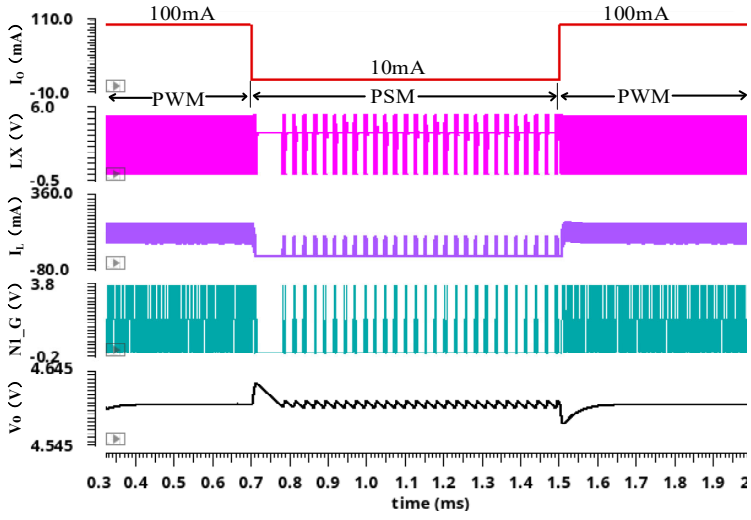


Figure 9. PWM/PSM automatic switching waveform

ISSN: 2472-3703 DOI: 10.6911/WSRJ.202503_11(3).0014

Fig. 9 shows the schematic diagram of PWM/PSM automatic switching, the load current I_O changes from 100 mA to 10 mA and back to 100 mA, and its operating frequency changes, and it can be clearly seen that the operating frequency under 10 mA is smaller than that under 300 mA, and the system can automatically switch between PWM mode and PSM mode.

According to the simulation results, the average input current I_{in} can be calculated, and the conversion efficiency of the system can be calculated by substituting into Equation (1) as shown in Fig. 10. It can be seen that the light load efficiency of the improved system is greatly improved.

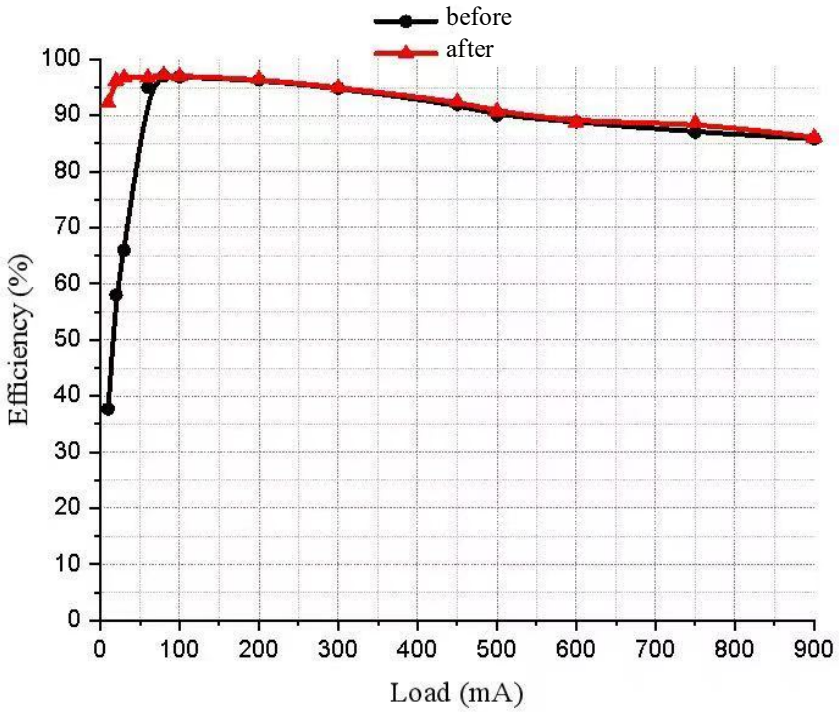


Figure 10. Conversion efficiency of the system

Table 1 lists the conversion efficiency of this paper compared with literature [5], literature [7], and literature [8]. Among them, literature [5] is a hybrid PWM/PFM modulation with load currents from 2 mA -500 mA and a ripple voltage of 33 mV, with a minimum conversion efficiency of 85 % and a maximum of 96 %, which is an improvement in light load efficiency, but the ripple voltage is too large. Literature [7].Using PWM/PFM auto switching mode, the load current range is 10 mA -40 mA. the maximum efficiency is 82 % and the minimum efficiency is 66 %. The light load efficiency is too low and the output voltage ripple is 55 mV, the ripple is too large to affect the stability of the circuit. Literature [8] uses DPWM/DPFM modulation with simple circuit structure. The maximum efficiency is up to 90 % and the minimum efficiency is 80 %, which has some improvement on the conversion efficiency, but the load current range from 1 μA to 3 mA is too small. Compared with the hybrid PWM/PSM modulation proposed in this paper, there is a wider load range of 10 mA-900 mA. the minimum conversion efficiency is 92.22 %, and the maximum conversion efficiency can be up to 97 %, which is a high conversion efficiency in the full load range. With a maximum ripple voltage of 7.28 mV, the circuits have low ripple and higher output voltage accuracy.

ISSN: 2472-3703 DOI: 10.6911/WSRJ.202503_11(3).0014

Table 1. Literature contrast

Note:"—" means not found.

parameters	Literature 5	Literature7	Literature 8	This article
technique	65 nm CMOS	0.18 μm CMOS	0.18 μm CMOS	0.18 μm BCD
control mode	PWM/PFM	PFM	DPWM/DPFM	PWM/PSM
C/uF	6.8	100	4.7	22
L/uH	10	1000	4.7	4.7
V_{IN}/V	2.1	3.3	0.6	3.7
V_{OUT}/V	1.5	1.1	0.45	4.6
Load current range/mA	2-500	10-40	0.001-3	10-900
efficiency/%	85-96	66-82	80-90.5	92.22-97
Overall map/$(mm)^2$	—	—	1.12	1.73
Maximum Ripple Voltage/mV	33	50	—	7.28
F	0.00028	0.006910	0.058951	0.000070

The value of F in Table 1 represents the comprehensive performance of the efficiency of the Boost converter:

$$F = \frac{|\eta_{Load}(\max) - \eta_{Load}(\min)|}{I_{Load}(\max) - I_{Load}(\min)} \bullet \frac{1}{\eta_{\max}} \tag{14}$$

where $\eta_{Load(max)}$ represents the maximum load efficiency, $\eta_{Load(min)}$ represents the minimum load efficiency, $I_{Load(max)}$ represents the maximum load current, $I_{Load(min)}$ represents the minimum load current, and η_{max} represents the maximum efficiency of the system. the smaller F represents the higher conversion efficiency of the system and the more stable it is.

7. CONCLUSION

Aiming at the uneven conversion efficiency of traditional boost-type DC-DC converter in the full load range, this paper proposes a combined method of over-zero detection technique and pulse width modulation (PWM)/periodic hopping modulation (PSM) automatic switching technique, which has been successfully applied to the boost-type peak current-mode-controlled DC-DC switching power supply management chip, realizing a comprehensive improvement of the efficiency from the light load to the heavy load. The results show that when the inductor current reaches zero, the current path from the output to the input can be cut off in time to avoid backflow of current and improve the conversion efficiency. At the same time, some cycles are skipped at small current loads, reducing the operating frequency.

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